AMENDMENTS TO THE CLAIMS:

The following claims replace all prior versions and listings of claims in the application:

1. (Currently amended) A serial scaleable bandwidth interconnect ~~bus~~ for interconnection of physical layer and link layer devices, comprising:

(a) an ADD Bus operative to receive signals from said link layer devices and direct them to said physical layer devices; and

(b) a DROP Bus operative to receive signals from said physical layer devices and direct them to said link layer devices; and

(c) an in-band communication channel for carrying only control and status signals through said DROP bus from said physical layer device to said Link Layer device and through said ADD Bus from said Link Layer device to said physical layer device

wherein said serial interconnect is capable of supporting a plurality of client tributaries.

~~wherein said serial scaleable bandwidth interconnect bus is capable of supporting a plurality of links; and~~

~~wherein, for one or more of said links, ADD Bus timing control information is conveyed from said physical layer to said link layer in-band of said DROP Bus and independently of other ones of said links~~.

2. (Currently amended) The interconnect ~~bus~~ according to claim 1, wherein ~~said~~ ADD Bus timing control information for each client is conveyed independently from said physical layer device to said Link Layer device using extended ~~conveyed from said physical layer device to said Link Layer device over said in-band communication channel by extended~~ 8B/10B ~~encoded~~ encoding.

3. (Currently amended) The interconnect ~~bus~~ according to claim 1, wherein said interface supports fractional links.

4. (Currently amended) The interconnect ~~bus~~ according to claim 1, wherein a bandwidth of each of said fractional links is an arbitrary rate up to a maximum of approximately 45MB/s.

5. (Currently amended) The interconnect ~~bus~~ according to claim 1, wherein said interface supports T1s, E1s, TVT1.5s, TVT2s, DS3s, E3s or fractional links.

6. (Currently amended) The interconnect ~~bus~~ according to claim 1, wherein said interface supports 336 T1s, 252 E1s, 336 TVT1.5s, 252 TVT2s, 12 DS3s, 12E3s or 12 fractional links.

7. (Currently amended) The interconnect ~~bus~~ according to claim 1, wherein said interface scales the number of client tributaries by increasing the serial interconnect rate in multiples of four.

8. (Currently amended) The interconnect ~~bus~~ according to claim 1, wherein said interface interconnects asynchronous and synchronous physical and link layer devices.

9. (Currently amended) The interconnect ~~bus~~ according to claim 1, wherein said interface is a ~~LVDS~~ serial differential interface.

10. (Canceled)

11. (Canceled)

12. (Currently amended) An apparatus for providing an ~~bus~~ interface for scaleable interconnection of physical layer and link layer devices, comprising:

(a) an ADD Bus operative to receive signals from said link layer devices and direct them to said physical layer devices; and

(b) a DROP Bus operative to receive signals from said physical layer devices and direct them to said link layer devices; and

(c) a full duplex in-band communication channel for carrying control and status signals through said DROP bus from said physical layer device to said Link Layer device and through said ADD Bus from said Link Layer device to said physical layer device

wherein said apparatus is capable of supporting a plurality of ~~links~~ client tributaries~~; and~~

~~wherein, for one or more of said links clients, ADD Bus timing control information is conveyed from said physical layer to said link layer in-band of said DROP Bus and independently of other ones of said links clients~~.

13. (Currently amended) The interconnect ~~bus~~ according to claim 12, wherein ~~said~~ ADD Bus timing control information for each client is conveyed independently using extended 8B/10B ~~enencoding~~d.

14. (Currently amended) The apparatus according to claim 12, wherein said ~~bus~~ interface is parallel and supports fractional links.

15. (Original) The apparatus according to claim 14, wherein a bandwidth of each of said fractional links is an arbitrary rate up to a maximum of approximately 45MB/s.

16. (Currently amended) The apparatus according to claim 12, wherein said ~~bus~~ interface supports T1s, E1s, TVT1.5s, TVT2s, DS3s, E3s or fractional links.

17. (Currently amended) The apparatus according to claim 12, wherein said ~~bus~~ interface supports 336 T1s, 252 E1s, 336 TVT1.5s, 252 TVT2s, 12 DS3s, 12E3s or 12 fractional links.

18. (Currently amended) The apparatus according to claim 12, wherein said ~~bus~~ interface scales the number of client tributaries by increasing the serial interconnect rate in multiples of four.

19. (Currently amended) The apparatus according to claim 12, wherein said ~~bus~~ interface interconnects asynchronous and synchronous physical and link layer devices.

20. (Currently amended) The apparatus according to claim 12, wherein said ~~bus~~ interface is a ~~LVDS~~ serial differential interface.

21. (Currently amended) The apparatus according to claim 12, wherein said interface is serial and said DROP Bus carries half of the full duplex in-band communications channel and said ADD Bus carries another half of said full duplex in-band communications channel ~~comprises an in-band half-duplex channel for conveying control information between said physical layer and said link layer~~.

22. (Canceled)

23. (Currently amended) A method for connecting one or more Physical Layer devices with one or more link Layer devices, comprising:

(a) providing an ADD Bus operative to receive signals from said link layer devices and direct them to said physical layer devices; and

(b) providing a DROP Bus operative to receive signals from said physical layer devices and direct them to said link layer devices; and

(c) providing a full duplex in-band communication channel for carrying control and status signals through said DROP bus from said physical layer device to said Link Layer device and through said ADD Bus from said Link Layer device to said physical layer device

wherein said ADD Bus and said DROP Bus are capable of supporting a plurality of ~~links~~ client tributaries~~; and~~

~~wherein, for one or more of said links, ADD Bus timing control information is conveyed from said physical layer to said link layer in-band of said DROP Bus and independently of other ones of said links~~.

24. (Currently amended) The interconnect ~~bus~~ according to claim 23, wherein said timing control information is conveyed independently for each client using extended 8B/10B ~~enen~~coding~~d~~.

25. (Original) The method of claim 23, wherein said ADD Bus and said DROP Bus support fractional links.

26. (Original) The method of claim 25, wherein a bandwidth of each of said fractional links is an arbitrary rate up to a maximum of approximately 45MB/s.

27. (Original) The method of claim 23, wherein said ADD Bus and said DROP Bus support T1s, E1s, TVT1.5s, TVT2s, DS3s, E3s or fractional links.

28. (Original) The method of claim 23, wherein said ADD Bus and said DROP Bus support 336 T1s, 252 E1s, 336 TVT1.5s, 252 TVT2s, 12 DS3s, 12E3s or 12 fractional links.

29. (Original) The method of claim 23, wherein said ADD Bus and said DROP Bus interconnect asynchronous and synchronous physical and link layer devices.

30. (Canceled)

31. (Currently amended) The method of claim 23, wherein said ADD Bus ~~comprises an~~ utilizes half of said in-band ~~half~~ full-duplex communications channel for conveying control and status signals from said physical layer devices to said link layer devices and said DROP Bus utilizes another half of said in-band, full-duplex communications channel for conveying control and status signals from said link layer devices to said physical layer devices.